IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Donald Craig Foster		
Assignee:	Amkor Technology, Inc.		
Title:	Stackable Lead Frame Package Using Exposed Internal Lead Traces		
Serial No.:	09/829,341	Filing Date:	April 9, 2001
Examiner:	Tuan T. Dinh	Group Art Unit:	2827
Docket No.:	M-9950 US		

San Jose, California
November 21, 2002

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RESPONSE TO OFFICE ACTION MAILED JUNE 19, 2002

Dear Sir:

Applicant responds to the Office Action mailed June 19, 2002 with the following amendments and remarks.

IN THE CLAIMS

Please amend claim 1 to read as follows. The changes to claim 1 are shown in an Appendix hereto. Below is a list of all of the now pending claims.

1. (Amended) A semiconductor die package, comprising:

conductive outer leads having first ends extending outside an encapsulant body of the package and second ends extending into an interior of the encapsulant body of the package;

conductive inner leads within the encapsulant body and having first ends extending to and electrically accessible through a first surface of the encapsulant body of the package; and

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a first die within the encapsulant body and electrically connected to the inner and outer leads.

2. The package of Claim 1, wherein the second ends of the outer leads do not extend beyond the first ends of the inner leads.

3. The package of Claim 1, wherein the second ends of the outer leads extend beyond the first ends of the inner leads.

4. The package of Claim 1, wherein the first surface is a bottom surface.

5. The package of Claim 4, further comprising a printed circuit board electrically coupled to the outer and inner leads.

6. The package of Claim 4, wherein the first ends of the inner leads are approximately co-planar with the first ends of the outer leads.

7. The package of Claim 4, wherein the first die is positioned above the inner leads.

8. The package of Claim 1, wherein the first surface is an upper surface.

9. The package of Claim 8, wherein the first die is positioned between the outer leads and the inner leads.

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10. The package of Claim 8, further comprising a second semiconductor die package coupled to the first die, wherein the second semiconductor die package comprises a second die and outer leads coupled to the second die.

11. The package of Claim 10, wherein the outer leads of the second die are electrically coupled to the inner leads of the first die.

12. The package of Claim 11, wherein the second die package is positioned over the first die.

13. The package of Claim 1, wherein the inner leads further comprise an interior portion electrically accessible through the first surface, and wherein the die is further electrically coupled to the interior portion.

14. The package of Claim 13, wherein the interior portion and the first ends of the inner leads and the first ends of the outer leads are electrically coupled to a printed circuit board.

33. The package of Claim 1, wherein the conductive inner leads are formed from an internal paddle area.

34. The package of Claim 33, further comprising means for securing and electrically isolating the conductive inner leads.

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35. The package of Claim 33, wherein the first die is attached to the internal paddle area.

36. The package of Claim 33, wherein the first ends of the inner leads are closer to the die than the first ends of the outer leads.

37. The package of Claim 33, wherein the first ends of the inner leads extend beyond the second ends of the outer leads.

38. The package of Claim 33, wherein the first ends of the inner leads do not extend beyond the second ends of the outer leads.

39. A semiconductor die package, comprising:

a lead frame having external leads;

internal leads electrically isolated from the external leads and secured to the lead frame;

means for securing and electrically isolating the internal leads from each other;

a die electrically coupled to the external leads and the internal leads; and

means for encapsulating the die and portions of the internal and external leads, wherein a first end of at least some of the internal leads is exposed through a surface of the means for encapsulating.

40. The package of Claim 39, wherein the internal leads are formed from an internal paddle area.

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41. The package of Claim 40, wherein the first ends of the internal leads are exposed through a bottom surface of the means for encapsulating.

42. The package of Claim 40, wherein the first ends of the internal leads are exposed through a top surface of the means for encapsulating.

43. The package of Claim 42, further comprising a second die package overlying the die package and electrically coupled to the internal leads of the die contained within the die package.

44. The package of Claim 40, wherein the ends of the internal leads are bent towards the surface of the means for coupling.

45. The package of Claim 40, wherein the external leads have first ends extending outside the means for encapsulating and second ends extending toward the die, and wherein the second ends of the external leads extend beyond the ends of the internal leads.

46. A semiconductor die package, comprising:

a die;

an enclosure protecting the die;

external leads each having a first and a second end, wherein the first ends extend beyond the enclosure and the second ends are electrically coupled to the die; and

internal leads having at least first ends exposed through the enclosure, wherein the die is electrically coupled to the internal leads, and wherein the internal leads are electrically isolated from the external leads.

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47. The package of Claim 46, wherein the first ends of the internal and external leads are approximately co-planar.

48. The package of Claim 46, where the first ends of the internal and external leads are located on opposite sides of the enclosure.

49. The package of Claim 48, further comprising a second die located over the die and electrically coupled to the first ends of the internal leads.

50. The package of Claim 46, wherein the first ends of the internal leads and the second ends of the external leads are interleaved.

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REMARKS

Please reconsider the application in view of the amendment to claim 1 and the following remarks.

I. Traverse of Examiner's Failure to Examine Certain Elected Claims

Referring to Paragraph 1 of the Office Action, the Examiner did not examine claims 39-41 and 46-47, on grounds that features of the claims were not present in Embodiment III, which is exemplified by Figure 3B. The Examiner's position is respectfully traversed.

Initially, the Examiner must note the statement in the specification, at page 5, line 4, that "Use of the same or similar reference numbers in different figures indicates same or like elements." The Specification proceeds to discuss Figs. 2, 3A, and 3B, wherein inner lead traces ("ILTs") 20 are discussed in detail. Both Figures 3A and Figure 3B show ILTs 20 exposed through encapsulant 34.

Regarding claim 39, and contrary to the Examiner's position, the feature of "wherein a first end of at least some of the internal leads is exposed through a surface of the means for encapsulating" is shown in the example of Figure 3B. In particular, inner lead traces ("ILTs") 20 are shown to be exposed through encapsulant 34 in Fig. 3B, and electrically coupled by solder 38 to printed circuit board 17. In fact, in this exemplary embodiment, not only is the outer end of the ILT 20 exposed, the inner end also is exposed. The text of the specification clearly supports the claim language:

> Fig. 3B is a side view of another embodiment of a lead frame package 10-2 with die 30. As noted above, die 30 is secured to ILT tape 33 by non-conductive film or paste 32 when tape 33 is placed on top of ILTs 20. In this embodiment, interior portions of ILTs 20 are also exposed through encapsulant 34, such as through an ILT pad 39. Die 30 can then be electrically connected to PCB 37 through OLTs 12, ILTs 20, and ILT pad 39 and solder 38. The additional connection using ILT pad 39 helps solve high frequency applications by creating low inductance signal paths through the bottom exposed ILT leads, with the exposed pad handling increased thermal needs due to the high frequency.

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See page 7, line 26 *et seq.* **as amended** in the Response to Office Action filed on April 8, 2002. Hence, claim 39's feature of "wherein a first end of at least some of the internal leads is exposed through a surface of the means for encapsulating" is shown in Figure 3B.

Regarding claim 46, the Examiner asserted that the feature of "internal leads having at least first ends exposed through the enclosure" is not shown in Figure 3B. This assertion is traversed for the same reasons stated for claim 39. In particular, ILTs 20 are shown exposed through encapsulant 34.

Accordingly, it is requested that the Examiner examine claims 39 and 46, and their dependent claims 40 and 41, and 47. Further, since the Examiner erred in not examining these claims, any rejection of the claims in a further Office Action must be non-final.

II. Rejection of claims 1-2, 4-7, 33-36 and 38

Claims 1-2, 4-7, 13-14, 33-36, and 38 were rejected under 35 USC 102(b) as anticipated by Liang et al. (U.S. Patent 5,332,864). Claim 1 is amended in a manner that distinguishes Liang et al. In particular, Liang et al. do not show at least the feature of "conductive inner leads having first ends extending to and electrically accessible through a first surface of the encapsulant body of the package." Support for the amendment is shown in Figure. 3B, and in the text quoted above regarding Figure 3B. Hence, the rejection is overcome.

CONCLUSION

The Examiner's refusal to examine certain claims, and rejection of other claims, are

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overcome. Please direct any comments or questions to the undersigned at (408) 487-1315.

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